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Date: August 8, 2005

Hui Chin Barnhill

In re application of: **Sun**

U.S. Serial Number: **10/750,752**

Filing Date: **January 2, 2004**

Our Reference Number: **250122-1140**

Confirmation No.: **1840**

Art Unit: **2815**

Examiner: **Fenty, Jess A.**

Title: **System for Integrating a Circuit on an Isolation Layer and Method Thereof**

Response to Office Action

Total Pages Transmitted (including cover sheet) - 14

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Wein-Town Sun
Serial No.: 10/750,752
Filed: 01/02/2004

Confirmation No. 1840
Group Art Unit: 2815
Examiner: FENTY, JESSE A

Title: **SYSTEM FOR INTEGRATING A CIRCUIT ON AN ISOLATION LAYER AND METHOD THEREOF**

TKHR REF. 250122-1140
TOP-TEAM REF. 0632-10326US

Certificate of Mailing
I hereby certify that this correspondence is being deposited with the United States Postal Service via facsimile to (571) 273-8330 on August 8, 2005.

Signature – Hui Chin Barnhill

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

In response to the Office Action dated December 16, 2004, a Response to which is due on or before 6/1/2005, please amend the above-identified application as follows:

Amendments to the Claims:

The listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (currently amended): A system for integrating circuitry on an isolation layer, comprising:

a plurality of isolation substrates, each isolation substrate having a circuit deposition region and a substrate-combining region;

a plurality of circuits formed on the circuit deposition regions;

a plurality of substrate-connecting elements formed to connect the substrate-combining regions; and

a plurality of electrical connecting elements formed to electrically connect the circuits formed on the different circuit deposition regions, wherein the circuit deposition region contacts the substrate-combining region on ~~different planes~~ more than one face thereof, and wherein at least two isolation substrates contact at respective substrate-combining regions.

2. (original): The system as claimed in claim 1, wherein the substrate-connecting elements are formed by heat fusing or laser.

3. (original): The system as claimed in claim 1, wherein the electrical connecting elements are flex print cables or gold lines.

4. (original): The system as claimed in claim 1, wherein the electrical connecting elements are formed by laser fusing.

5. (original): The system as claimed in claim 1, wherein the materials of the isolation substrates are different.

6. (canceled)

7. (original): The system as claimed in claim 1, wherein the materials of the isolation substrates are plastic or glass.

8. (Previously presented): A method for integrating a system on an isolation layer, comprising the following steps:

providing a first isolation substrate including a first circuit deposition region and a first substrate-combining region, and a second isolation substrate including a second circuit deposition region and a second substrate-combining region;

forming a first circuit and a second circuit respectively on the first circuit deposition region and the second circuit deposition region;

contacting the first substrate-combining region and the second substrate-combining region;

forming a plurality of substrate-connecting elements for connecting the first substrate-combining region to the second substrate-combining region; and

forming a plurality of electrical connecting elements to electrically connect the first circuit and the second circuit.

9. (Original): The method for integrating a system on an isolation layer as claimed in claim 8, wherein the substrate-connecting elements are formed by heat fusing or laser.

10. (Original): The method for integrating a system on an isolation layer as claimed in claim 8, wherein the electrical connecting elements are flex print cables or gold lines.

11. (Original): The method for integrating a system on an isolation layer as claimed in claim 8, wherein the electrical connecting elements are formed by laser fusing.

12. (Original): The method for integrating a system on an isolation layer as claimed in claim 8, wherein the first circuit and the second circuit are packed by different packaging methods.

13. (Original): The method for integrating a system on an isolation layer as claimed in claim 8, wherein the material of the first isolation substrate and the second isolation substrate is plastic.

14. (Original): The method for integrating a system on an isolation layer as claimed in claim 8, wherein the material of the first isolation substrate and the second isolation substrate are glass.

15. (Original): A method for integrating a system on an isolation layer, comprising the following steps:

providing a first isolation substrate and a second isolation substrate respectively including a first circuit deposition region and a second circuit deposition region;

forming a plurality of first circuits and a plurality of second circuits respectively on the first circuit deposition region and the second circuit deposition region;

cutting the first isolation substrate and the second isolation substrate, wherein the cut first isolation substrate comprises single first circuit and a first substrate-combining region, and the cut second isolation substrate comprises a single second circuit and a second substrate-combining region;

forming a plurality of substrate-connecting elements for connecting the cut first isolation substrate to the cut second isolation substrate, wherein the first substrate-combining region contacts the second substrate-combining region; and

forming a plurality of electrical connecting elements to electrically connect the single first circuit and the single second circuit.

16. (Original): The method for integrating a system on an isolation layer as claimed in claim 15, wherein the substrate-connecting elements are formed by heat fusing or laser.

17. (Original): The method for integrating a system on an isolation layer as claimed in claim 15, wherein the electrical connecting elements are flex print cables or gold lines.

18. (Original): The method for integrating a system on an isolation layer as claimed in claim 15, wherein the electrical connecting elements are formed by laser fusing.

19. (Original): The method for integrating a system on an isolation layer as claimed in claim 15, wherein the material of the first isolation substrate is plastic.

20. (Original): The method for integrating a system on an isolation layer as claimed in claim 15, wherein the material of the second isolation substrate is glass.

21. (currently amended): A method for integrating a system on an isolation layer, comprising the following steps:

providing a first isolation substrate including a first circuit deposition region and a first substrate-combining region, and a second isolation substrate including a second circuit deposition region and a second substrate-combining region, wherein the materials of the first and second isolation substrates are different;

forming a first circuit and a second circuit respectively on the first circuit deposition region and the second circuit deposition region~~, wherein the first circuit and the second circuit are packed by different packaging methods~~;

forming a plurality of substrate-connecting elements for connecting the first substrate-combining region to the second substrate-combining region; and

forming a plurality of electrical connecting elements to electrically connect the first circuit and the second circuit.

IN THE DRAWINGS:

FIG. 4 has been amended by replacing the label "22B" on the left side with "24B". Support for the amendment is shown on page 5, lines 20-22 in the specification, "the isolation substrates 20A and 20B are cut along cutting lines 24A and 24B".

Attachments

Annotated Drawing Sheet

Replacement Drawing Sheet

REMARKS

Allowable Subject Matter

The Examiner is thanked for the thorough examination of this application and the allowance of claims 8-20.

Claims 1-5 and 7-21 remain in this application. Claim 1 is amended herein by replacing the term "on different planes" to "on more than one face thereof" to overcome 112 rejections. In addition, claim 1 has been amended by adding "at least two isolation substrates contact at respective substrate-combining regions". Support for the amendment is shown at least in page 6, lines 4-6, "FIGs. 5A and 5B show the circuit blocks connected by the electrical connecting elements, wherein the isolation substrates are in contact".

Claim 21 has been amended to incorporate the limitations recited in Claim 5, and to cancel delete "the first circuit and the second circuit are packed by different packaging methods".

35 U.S.C. 112

Claims 1-5 and 7 were tentatively rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. In this regard, the Office Action alleged that, regarding claim 1, the specification does not explain what is mean by the term "on different planes."

Claim 1 has been amended by replacing the term "on different planes" to "on more than one face thereof". Support for the amendment is shown in page 5, lines 23-27 and FIG. 4 of the specification, "The top surface of the cut isolation substrate 20B is a *circuit deposition region 21*, which is deposited on the CPU block, and the side surfaces 26 of the cut isolation substrate 20B contiguous to the circuit deposition region 21 are *substrate-combining regions*".

Accordingly, the 112 rejection has been rendered moot by the amendment to claim 1.

35 U.S.C. 102(b)

Claims 1-2, 4, 7 and 21 were tentatively rejected under 35 U.S.C. 102(b) as allegedly anticipated by Kaoth et al. (U.S. 5,963,785). For at least the reasons set for below, Applicant disagrees and requests reconsideration of the rejection.

Claim 1 recites:

> 1. A system for integrating circuitry on an isolation layer, comprising:
> ***a plurality of isolation substrates, each isolation substrate having a circuit deposition region and a substrate-combining region***;
> a plurality of circuits formed on the circuit deposition regions;
> a plurality of substrate-connecting elements formed to connect the substrate-combining regions; and
> a plurality of electrical connecting elements formed to electrically connect the circuits formed on the different circuit deposition regions, wherein the circuit deposition region contacts the substrate-combining region on more than one face thereof, ***and wherein at least two isolation substrates contact at respective substrate-combining regions.***

(*Emphasis added.*)

Kaoth does not teach or suggest at a system having at least two isolation substrates, wherein the at least two isolation substrates contact at respective substrate-combining regions. As illustrated in FIG. 3 of Kaoth, the first substrate-combining region of substrate 9 does not contact the second substrate-combining region of substrate 11.

For this reason, claim 1 is allowable over the cited reference. Insofar as claims 2-5 and 7, depend from claim 1 and its related claims, they are also allowable.

Claim 21 recites:

> 21. A method for integrating a system on an isolation layer, comprising the following steps:
> providing a first isolation substrate including a first circuit deposition region and a first substrate-combining region, and a second isolation substrate including a second circuit deposition region and a second substrate-combining

region, wherein the materials of the first and second isolation substrates are different;

forming a first circuit and a second circuit respectively on the first circuit deposition region and the second circuit deposition region;

forming a plurality of substrate-connecting elements for connecting the first substrate-combining region to the second substrate-combining region; and

forming a plurality of electrical connecting elements to electrically connect the first circuit and the second circuit.

(*Emphasis added.*)

Kaoth does not teach or suggest the materials of the first and second isolation substrates being different, as specifically claimed in claim 21. For at least this reason, claim 21 is allowable over the cited reference.

Conclusion

For the reasons as described above, all pending claims are now in condition for allowance. Applicant thanks the Examiner for his thorough review of the present application and his allowance of claims 8-20.

Withdrawal of the rejections and allowance of all claims, as now amended, are respectfully requested. Applicant has made every effort to place the present application in condition for allowance. It is therefore earnestly requested that the present application, as a whole, receive favorable consideration and that all of the claims be allowed in their present form.

Should Examiner feel that further discussion of the application and the Amendment is conducive to prosecution and allowance thereof, please do not hesitate to contact the undersigned at the address and telephone listed below.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: _____
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Annotated Sheet

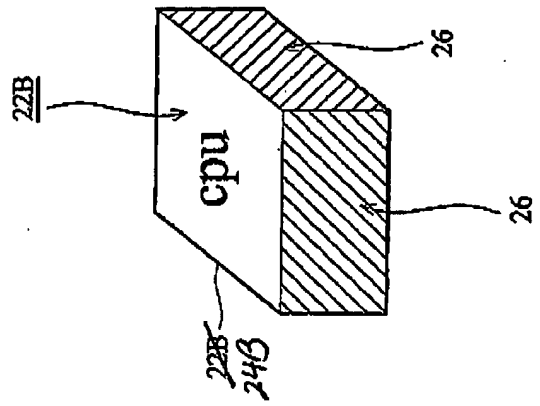

FIG. 4

Replacement Sheet

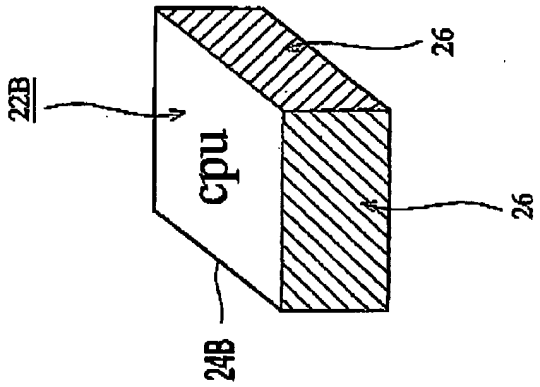

FIG. 4